FULL LISTING OF CLAIMS

1. (Currently Amended) A method of fabricating a portion of a memory cell, said method comprising:

forming an insulating layer over a substrate;

forming a trench in said insulating layer;

lining said trench with a first barrier layer ~~to a first conductive material~~;

forming ~~said~~ a first conductive layer in said lined trench;

planarizing an upper surface of said barrier and said first conductive layers with said surface of said insulating layer;

forming a second layer of a ~~second~~ conductive material over said barrier and said first conductive layers; and

removing an upper portion of said second conductive layer to substantially flatten an upper surface of said second conductive layer while leaving a lower portion of said second conductive layer intact over said first conductive layer and said barrier layer.

2. (original) The method of claim 1 wherein said first barrier layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

3. (Currently Amended) The method of claim 1 wherein said second conductive ~~layers~~ layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

4. (original) The method of claim 1 wherein said second conductive layer is a resistive material.

5. (original) The method of claim 1 wherein said first and second conductive layers are selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

6. (original) The method of claim 1 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

7. (original) The method of claim 1 wherein said first barrier layer is formed to a thickness of about 5 nm to about 10 nm.

8. (original) The method of claim 1 wherein said second conductive layer is formed to a thickness of about 5 nm to about 20 nm.

9. (Currently Amended) The method of claim 1 wherein the step of removing an ~~said~~ upper portion of said second conductive layer ~~is removed by~~ comprises performing a chemical mechanical polishing on said upper surface.

10. (original) A method of fabricating a portion of a memory cell, said method comprising:

forming a first conductor in a trench provided in an insulating layer;

flattening an upper surface of said insulating layer and said first conductor, said flattening leaving a roughened upper surface of said conductor;

forming a material layer over said flattened upper surface of said insulating layer and said first conductor; and

flattening an upper portion of said material layer while leaving intact a lower portion of said material layer over said insulating layer and said first conductor.

11. (original) The method of claim 10 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW),titanium nitride (TiN) and chromium (Cr).

12. (original) The method of claim 10 wherein said material layer is a resistive material.

13. (original) The method of claim 10 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO2, Si3N4 and polyimide.

14. (original) The method of claim 10 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

15. (original) The method of claim 10 wherein said upper portion of said material layer is flattened by chemical mechanical polishing.

16. (Currently Amended) A method of fabricating a portion of a memory cell, said method comprising:

forming a ~~first conductor~~ conductive layer over an insulating layer on ~~of~~ a substrate;

flattening an upper surface of said conductive layer ~~layers~~, said flattening leaving at least a partially roughened upper surface of said conductive layer;

forming a material layer over said flattened upper surface of said conductive layer ~~layers~~; ~~and~~

flattening an upper portion of said material layer ~~while leaving intact a lower portion of said material layer over said conductive layer~~; and

forming at least one magnetic layer over said flattened upper portion of said material layer.

17. (original) The method of claim 16 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

18. (original) The method of claim 16 wherein said material layer is a resistive material.

19. (original) The method of claim 16 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

20. (original) The method of claim 16 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

21. (original) The method of claim 16 wherein said upper portion of said material layer is flattened by chemical mechanical polishing.

22-39 **(CANCELED).**

40. (New) The method of claim 16 wherein the step of forming at least one magnetic layer over said flattened portion of said material layer comprises forming layers of a memory element stack.

41. (New) The method of claim 16 further comprising the step of etching said at least one magnetic layer everywhere except an area where a memory element stack is to be formed.

42. (New) The method of claim 16 further comprising the step of forming at least one non-magnetic layer over said at least one magnetic layer.